**Carleton University**

**Department of Systems and Computer Engineering**

**SYSC 3006 (Computer Organization) Summer 2020**

**Lab / Assignment 1 – Answering file**

### Question 1 [0.5-mark]

What is the minimum ROM Address Bit Width needed to implement Table 1, and why?  
*Answer in this space:*

### Question 2 [0.5-mark]

What is the minimum ROM Data Bit Width needed to implement Table 1, and why?  
*Answer in this space:*

### Question 3 [1-mark]

Fill in the following table; it is the content of your FSM ROM that you are going to implement.

|  |  |  |
| --- | --- | --- |
| Address | DATA content (binary) | DATA content (Hex) |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |

Table 2 - Lab1 ROM content

### Question 4 [3-mark]

* 1. [0.5-mark] Show here a screenshot of your final Logisim circuit for your implementation.

*Insert your image in this space:*

[0.5-mark]A short description of how the component attributes have been configured to meet the lab requirements.  
*Answer here:*

* 1. [2-mark] Including this document, submit your Logisim lab1 file circuit (.circ) in a zip folder. Also insert below a screenshot of your Log table (0.5-mark for the Log table and 1.5-mark for a circuit working properly and respecting the design specifications described in this statement).

*Insert your image in this space:*

*Now save this document as PDF and do not forget to include your .circ file with your submission!*

# Submission deadline

Must be submitter on cuLearn, locate (Assignment 1 submission) and follow instructions, submission exact deadline (date and time) is displayed clearly with the Assignment 1 submission on cuLearn.

***Note: If you have any question please contact your respective group TA (see TA / group information posted on cuLearn).***

Good Luck